19-3025; Rev 0; 11/03

EVALUATION KIT AVAILABLE

Quad-Output LNA with AGC for Cable TV Applications

General Description

The MAX3558 broadband quad-output low-noise amplifier (LNA) is designed for digital set tops and digital terrestrial applications. The LNA covers a 50MHz to 878MHz input frequency range, while integrating a separate automatic gain-control (AGC) function with over 30dB of control range for each of four balanced outputs. Each output has its own shutdown control to reduce power consumption when not used. The MAX3558 also includes a power detector that can be used to close the loop on any of the AGCs to prevent overload conditions. The LNA's attack point is adjustable with an external resistor. The MAX3558 is available in a very small 28-pin QFN package with exposed paddle (EP).

Applications

Digital Set-Top Boxes

Digital Terrestrial Receivers

Tuner Preamps

Features

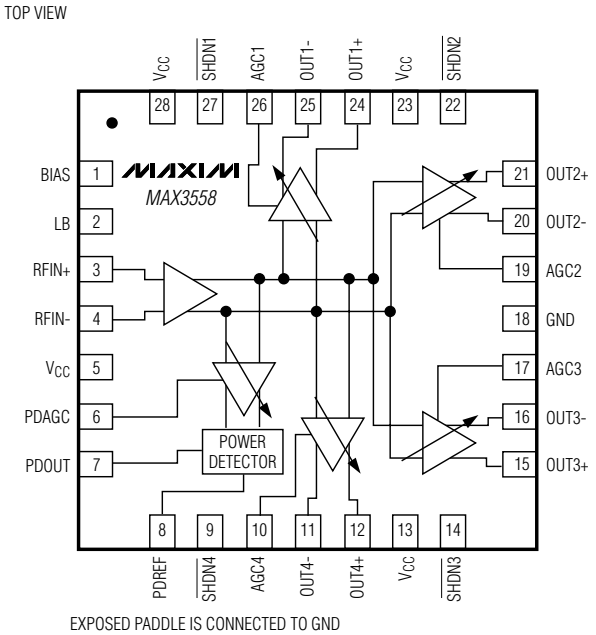
- **Quad Outputs with Independent AGCs and Shutdown**
- **50MHz to 878MHz Broadband Operation**
- **Integrated Power Detector**
- **High Linearity: 15.6dBm IIP3**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3558CGI	0°C to +70°C	28 QFN-EP* (5mm x 5mm)

**EP = Exposed paddle.*

Pin Configuration/Functional Diagram



Quad-Output LNA with AGC for Cable TV Applications

ABSOLUTE MAXIMUM RATINGS

V_{CC}, OUT_ _ to GND .....-0.3V to + 6.3V
BIAS, LB, RFIN_, PDAGC, PDOUT, PDREF, $\overline{SHDN}$_, AGC_ to GND .....-0.3V to (V_{CC} + 0.3V)
OUT_ _ Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-Pin QFN.....2.1W

Operating Temperature Range.....0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering ,10s) .....+300°C

CAUTION! ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.25V, no RF signal applied, R_{BIAS} = 1.1kΩ, R_{PDREF} = 10kΩ, L_{LB} = 82nH, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		4.75		5.25	V
Supply Current	Four outputs active, $V_{AGC\_}$ = 3V		241	287	mA
	Three outputs active, $V_{AGC\_}$ = 3V		206	245	
	Four outputs active, 10dB gain reduction		306	366	
	Four outputs active, $V_{AGC\_}$ = 0.5V		329	396	
	Four outputs shut down		103	121	
Power-Detector Output Current	PDOUT = V_{CC} - 0.5V	1			mA
	PDOUT = 0.5V	-0.8			
Analog Input Current	AGC_, PDAGC = 0 to 5V	-100		+100	µA
Logic-Low Input Voltage				0.8	V
Logic-High Input Voltage		2.0			V
Logic Input Current		-100		+10	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.25V, f_{RFIN} = 50MHz to 878MHz, 75Ω system impedance, $V_{AGC\_}$ = 3V, $V_{\overline{SHDN\_}}$ = V_{CC}, R_{BIAS} = 1.1kΩ, R_{PDREF} = 10kΩ, L_{LB} = 82nH, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = 5V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	Gain specification is met across the frequency band	50		878	MHz
Voltage Gain	Differential output load, maximum gain (Note 2)	4.0	6.8	9.3	dB
	Differential output load, $V_{AGC\_}$ = 0.5V, minimum gain		-27.6	-15.7	
Gain Flatness	50MHz to 878MHz		±0.4		dB
Noise Figure	Worst case across band, 75Ω source, at maximum gain		8.4	9.9	dB
Input P1dB Compression Point	Maximum gain	-1.1			dBm
	10dB gain reduction	+1.3			
Input 3rd-Order Intercept Point (IIP3) (Note 3)	Maximum gain, P_{IN} = -9dBm		14.4		dBm
	10dB gain reduction, P_{IN} = -9dBm (Note 2)		15.6		
Input 2nd-Order Intercept Point (IIP2) (Note 3)	Maximum gain, P_{IN} = -9dBm		+45.9		dBm
	10dB gain reduction, P_{IN} = -9dBm (Note 2)	+29.5			
Input Return Loss	Any gain setting		9		dB
Output Return Loss	75Ω differential output load	8			dB
OUT_ to RFIN Isolation		65			dB
RFIN to OUT_ Shutdown Isolation	VGA in shutdown, f_{RFIN} = 54MHz to 72MHz	40			dB
Output-to-Output Isolation	Between any two outputs	45			dB
Power-Detector Operating Range (per Channel)	f_{RFIN} = 50MHz to 878MHz (Note 4)	-3		+17	dBmV
AGC Attack Range (per Channel)	R_{PDREF} = 800Ω to 12kΩ, flat input of 130 channel loading (Notes 4, 5)	-3		+6	dBmV
AGC Attack Accuracy (per Channel)	130 channel loading (Notes 2, 4)	-2.2		+2.2	dBmV
Attack Point Variation	Any one output in shutdown mode (Note 4)	-0.5		+0.5	dBm
AGC Attack Slope	Change of POUT_ over 12dB change in P_{RFIN} after reaching AGC attack point (Notes 2, 4)	-2		+2	dB

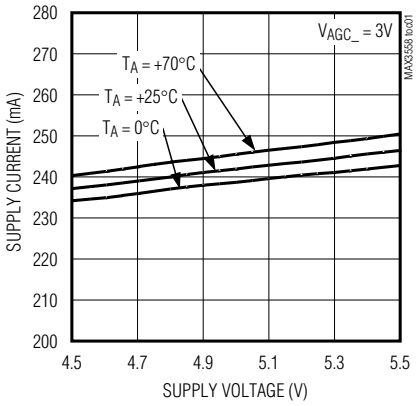
Note 1: Guaranteed by design and characterization.
Note 2: Guaranteed by production test.
Note 3: Measured with two input tones (f_1 = 800MHz, f_2 = 845MHz).
Note 4: PDOUT connected to PDAGC and AGC_.
Note 5: P_{IN} is single-tone equivalent to 130 channel loading.

Quad-Output LNA with AGC for Cable TV Applications

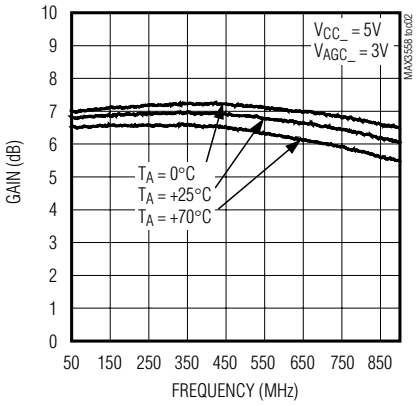
Typical Operating Characteristics

(MAX3558 EV kit, V_{CC} = 5V, f_{RFIN} = 50MHz to 878MHz, $V_{AGC\_}$ = 3V, $V_{\overline{SHDN}\_}$ = V_{CC}, R_{BIAS} = 1.1kΩ, R_{PDREF} = 10kΩ, L_{LB} = 82nH, T_A = +25°C, unless otherwise noted.)

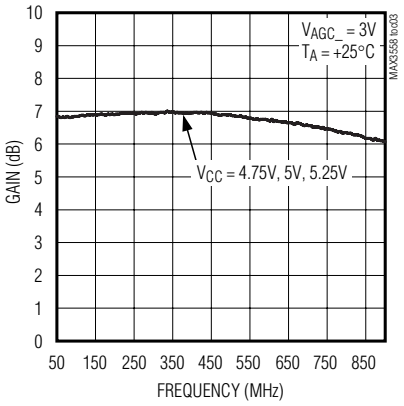
SUPPLY CURRENT vs. SUPPLY VOLTAGE



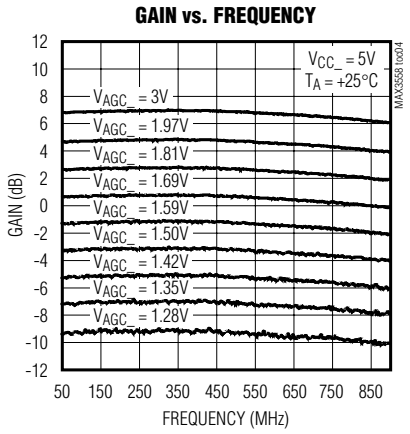
GAIN vs. FREQUENCY



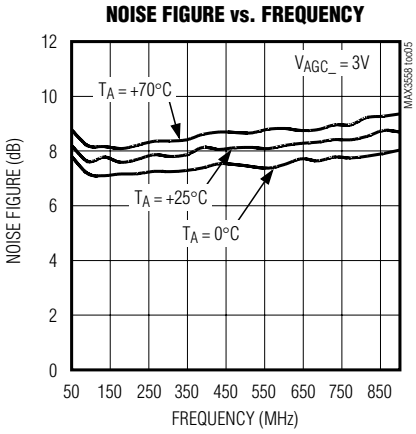
GAIN vs. FREQUENCY



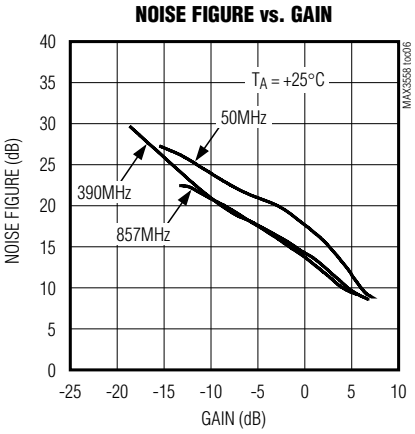
GAIN vs. FREQUENCY



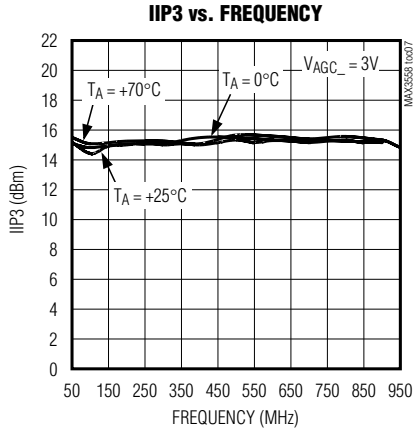
NOISE FIGURE vs. FREQUENCY



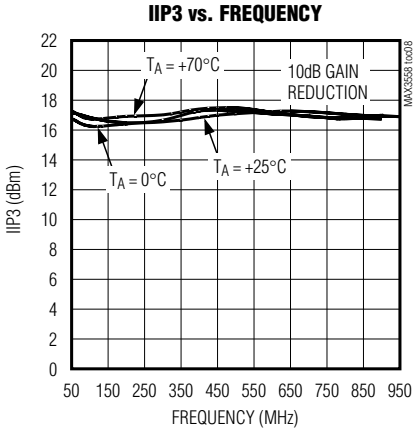
NOISE FIGURE vs. GAIN



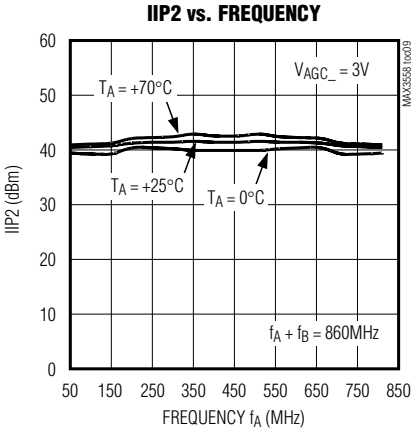
IIP3 vs. FREQUENCY



IIP3 vs. FREQUENCY



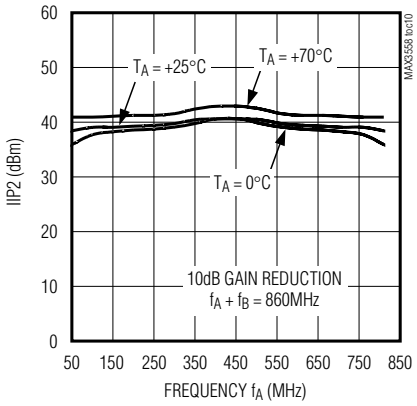
IIP2 vs. FREQUENCY



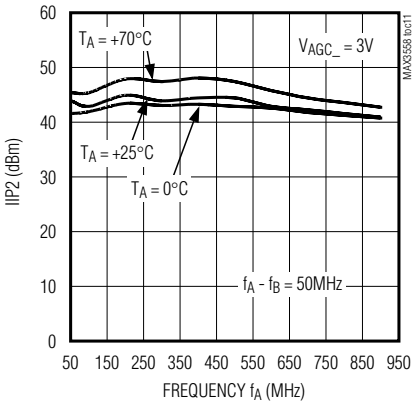
Typical Operating Characteristics (continued)

(MAX3558 EV kit, V_{CC} = 5V, f_{RFIN} = 50MHz to 878MHz, $V_{AGC\_}$ = 3V, $V_{\overline{SHDN}\_}$ = V_{CC}, R_{BIAS} = 1.1kΩ, R_{PDREF} = 10kΩ, L_{LB} = 82nH, T_A = +25°C, unless otherwise noted.)

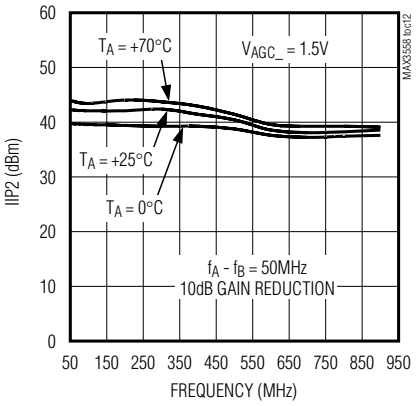
IIP2 vs. FREQUENCY



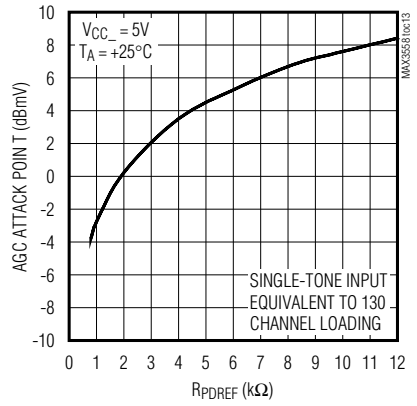
IIP2 vs. FREQUENCY



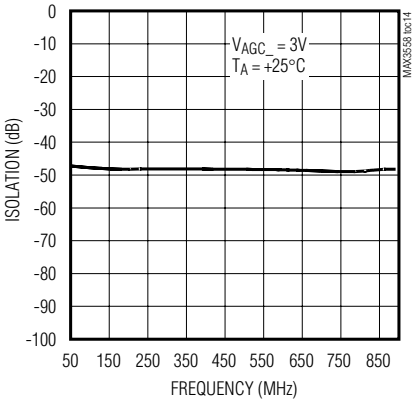
IIP2 vs. FREQUENCY



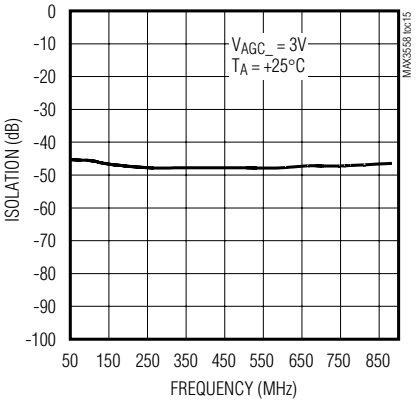
AGC ATTACK POINT vs. R_{PDREF}



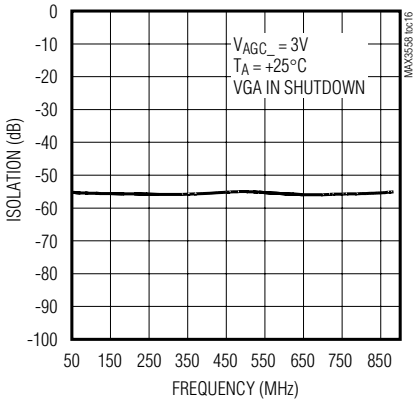
PORT-TO-PORT ISOLATION vs. FREQUENCY



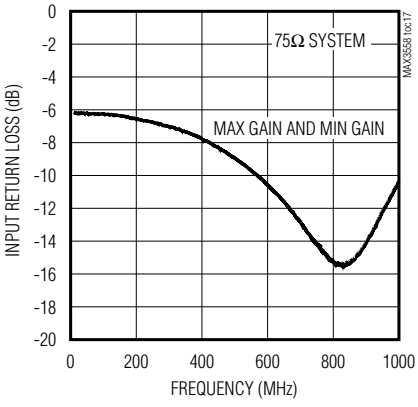
OUTPUT TO RFIN ISOLATION vs. FREQUENCY



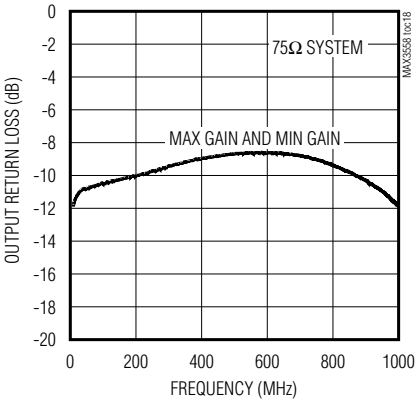
RFIN TO OUTPUT ISOLATION vs. FREQUENCY



INPUT RETURN LOSS vs. FREQUENCY



OUTPUT RETURN LOSS vs. FREQUENCY



Quad-Output LNA with AGC for Cable TV Applications

Pin Description

PIN	NAME	FUNCTION
1	BIAS	External Bias. Connect an external 1.1kΩ ±1% resistor to set the bias current.
2	LB	Inductor Bias. Connect an 82nH inductor to ground for proper operation.
3, 4	RFIN+, RFIN-	Differential LNA RF Input. Requires external DC-blocking capacitors. For single-ended input, AC-couple RFIN- to GND.
5, 13, 23, 28	V_{CC}	V_{CC} Power Supply. Bypass each V_{CC} with a 0.01µF capacitor to ground as close to the device as possible.
6	PDAGC	Power-Detector AGC Input. Connect PDAGC to PDOUT for closed-loop AGC control.
7	PDOUT	Power-Detector Output. PDOUT can be connected to AGC_ for closed-loop operation. PDOUT bandwidth is set by an external capacitor.
8	PDREF	Power-Detector Reference Input. Connect an external resistor to ground to lower the attack point.
9	$\overline{SHDN4}$	Shutdown Input 4. Drive logic low to disable OUT4_ and AGC4. Drive logic high for normal operation.
10	AGC4	Automatic Gain-Control Input 4. AGC4 sets the gain of the LNA output OUT4_.
11, 12	OUT4-, OUT4+	Differential LNA Output 4. Requires external DC-blocking capacitors.
14	$\overline{SHDN3}$	Shutdown Input 3. Drive logic low to disable OUT3_ and AGC3. Drive logic high for normal operation.
15, 16	OUT3+, OUT3-	Differential LNA Output 3. Requires external DC-blocking capacitors.
17	AGC3	Automatic Gain-Control Input 3. AGC3 sets the gain of the LNA output OUT3_.
18	GND	Ground
19	AGC2	Automatic Gain-Control Input 2. AGC2 sets the gain of the LNA output OUT2_.
20, 21	OUT2-, OUT2+	Differential LNA Output 2. Requires external DC-blocking capacitors.
22	$\overline{SHDN2}$	Shutdown Input 2. Drive logic low to disable OUT2_ and AGC2. Drive logic high for normal operation.
24, 25	OUT1+, OUT1-	Differential LNA Output 1. Requires external DC-blocking capacitors.
26	AGC1	Automatic Gain-Control Input 1. AGC1 sets the gain of the LNA output OUT1_.
27	$\overline{SHDN1}$	Shutdown Input 1. Drive logic low to disable OUT1_ and AGC1. Drive logic high for normal operation.
—	EP	Exposed Paddle Ground. The exposed paddle must be soldered to GND for DC and RF return and better thermal dissipation.

Detailed Description

The MAX3558 broadband LNA consists of a single input and four independent outputs. Each output has its own AGC and shutdown function. The LNA covers the 50MHz to 878MHz cable and terrestrial TV frequency range. In addition, the device includes a power detector that can be used to control the AGC function. The MAX3558 is available in a space-saving 28-pin QFN package.

Broadband LNA

The broadband LNA input is differential and internally matched to 75Ω. The LNAs require only DC-blocking capacitors while maintaining 6dB input return loss. The input stage drives four variable-gain amplifiers (VGAs).

RF VGAs

The RF VGAs feature an independent gain-control range of more than 30dB. The voltage applied at the AGC pin controls the gain. Minimum gain corresponds to AGC_ voltage of 0.5V and maximum gain corresponds to AGC_ voltage of 3V. AGC inputs can be driven from a demodulator's AGC output, which normally controls a tuner's RF AGC, or from the MAX3558's on-chip power detector. Should an overload condition occur, the closed-loop AGC circuitry continues to reduce the gain to ensure good distortion performance. For optimum distortion and signal-to-noise ratio (SNR) performance, set the AGC attack point between +3dBmV to +5dBmV with an external resistor connected to PDREF.

The VGA outputs are differentially balanced to achieve good IIP2 performance while providing at least 8dB return loss. The outputs are internally matched to 75Ω. Each output has its own shutdown pin. The shutdown function disables the selected VGA to reduce power consumption while also providing significant input-to-output isolation.

Power Detector

The MAX3558 includes on-chip power-detector circuitry that can be used to control the gain of any of the four RF VGAs to prevent overload conditions. The broadband power detector allows the circuit to automatically limit the gain when the total input power reaches a set level. This level, or attack point, is user adjustable with an external resistor connected to PDREF. Because the power detector has a broadband frequency response, the MAX3558 allows the RF AGC attack point to be set according to the total input power, as opposed to the tuned channel. This minimizes the linearity requirements while ensuring good SNR and distortion performance. The on-chip power detector allows the device to be used with multiple tuners without complicated RF AGC circuitry.

Applications Information

Using a Power Detector to Set the Attack Point

The on-chip power detector can be used closed loop as an automatic gain-control circuit for any one (or all) of the LNA outputs. The power detector is designed for the attack point to be set in the -3dBmV to +6dBmV range with the resistor R_{PDREF}. The resistor value is chosen between 800Ω and 12kΩ. A larger resistor value sets a higher output attack point. See Attack Point vs. R_{PDREF} in the *Typical Operating Characteristics*.

For on-chip closed-loop operation, PDAGC must be connected to PDOUT. Connect a 0.1µF capacitor from PDOUT to ground for filtering. The PDOUT can be connected to any one of the AGC input pins to prevent overload conditions.

Bias Current

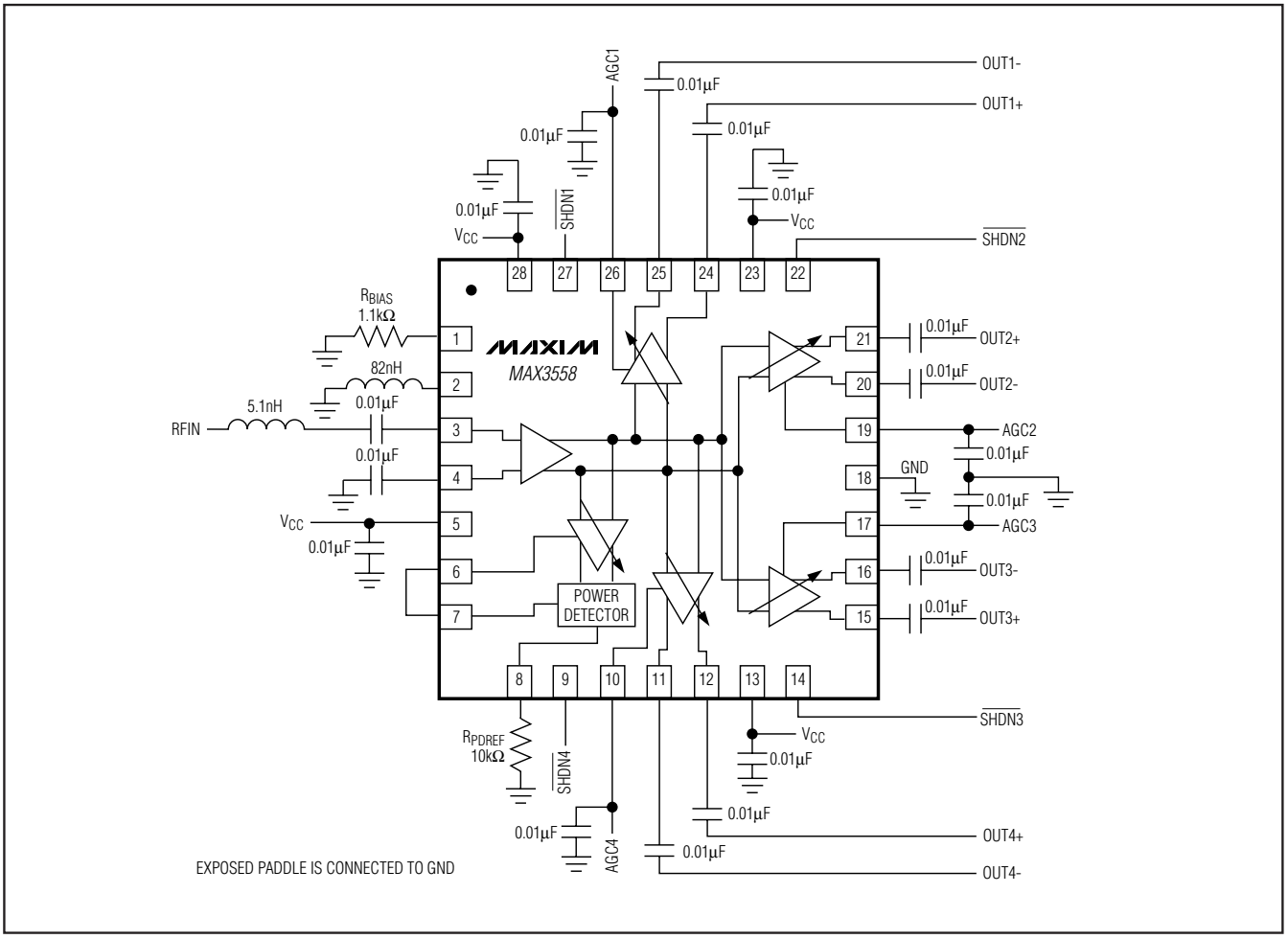
The MAX3558 uses an external resistor for adjusting the biasing current. A resistor, R_{BIAS}, connected from BIAS to ground sets the supply current. To achieve the specified distortion and noise-figure performance, set R_{BIAS} to 1.1kΩ ±1%.

Layout Considerations

The EV kit serves as a guide for PC board layout. Keep RF signal lines as short as possible to minimize losses and radiation. Use controlled impedance on all high-frequency traces. For proper operation, solder the exposed paddle evenly to the ground plane. Use abundant vias beneath the exposed paddle for maximum heat dissipation. Use abundant ground vias between RF traces to minimize undesired coupling. Each V_{CC} pin must have its own bypass capacitor placed close to the pin.

Quad-Output LNA with AGC for Cable TV Applications

Typical Application Circuit



Chip Information

TRANSISTOR COUNT: 4930

PROCESS: Bipolar

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

REFERENCE: 28-pin QFN 5mm × 5mm

PACKAGE CODE: G2855-2